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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/434,654	11/05/1999	KEVIN J RYAN	303.306US4	4209

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EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
2186	10

DATE MAILED: 03/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/434,654	Ryan
Examiner	**Art Unit**
B. James Peikari	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jan 18, 2002*

2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *13-16 and 32-60* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *13-16 and 32-60* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Nov 5, 1999* is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a data in buffer, a data out buffer, a column decoder, and a row decoder must be shown for each memory device (i.e., DRAM) or the feature(s) canceled from the claim(s). No new matter should be entered.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description: data bus 120. Correction is required.

Specification

3. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

With regard to the paragraph beginning at page 8, line 8, upon further inspection, it appears that this should read "memory system 100 has eight memory subsystems, each with eight memory devices 135 (i.e., N times M equals sixty-four)".

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 13-16 and 32-60 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. There is no mention in the specification of several critical features of the claims, specifically, that "each memory device contains a data in and a data out buffer, a column decoder and a row decoder".

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 13-16 and 32-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al., U.S. 5,875,452, in view of Bechtolsheim et al., U.S. 5,270,964.

Katayama et al. teach the claimed invention in a memory system (*note especially Figure 9*) comprising:

a memory controller (*note memory controller 17, via controller 70*) with a unidirectional command and address bus (*note that the address and control lines from controller 70 to the decoders are all unidirectional*),

a bidirectional data bus (*note that data line 56 is bidirectional*), a plurality of memory devices, such as eight, (*note the use of up to sixteen exemplary DRAM devices 22*),

a shared command buffer (*note the registers A and B in controller 70, which are connected to each of the plurality of memory devices 22, as explained in column 26, lines 56-57*) coupled between the command and address bus (*18; note that bus 18 comprises, in part, a control bus and an address bus*) and the plurality of memory devices (*22*) for receiving and latching commands and addresses, and

a shared data buffer (*note data buffer 78*) connected between the plurality of memory devices (*22*) and the bidirectional data bus (*18; note that bus 18 comprises, in part, a data bus*) for receiving and latching read data or write data.

As for the claimed packet protocol which required the particular insertion of delays along the processing path, this was taught by the pipeline protocol disclosed in column 2, lines 34 et seq. and column 20, line 6.

As for the feature of each memory device containing a column decoder and a row decoder, note column 26, lines 51-57.

As for the feature of each memory device containing a data in buffer and a data out buffer, such was not specifically mentioned in the Katayama et al. system. However the benefits of adding additional levels of buffer hierarchies was well known at the time of the invention. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include data in and data out buffers for each of the memory devices 22 in the Katayama et al. system, since these buffers would have made the timing of the transfer operations to and from the shared buffers more efficient (by latching the data, control or address bits so that such protocols as time sharing could be utilized), especially considering the highly parallel nature of the Figure 9 embodiment of the Katayama et al. system.

At this point it is apparent that storage device 16 of Katayama et al. teaches (or suggests, in the case of the data in buffer and data out buffer) each and all of the features of *one* of applicant's memory "modules" 130.N. On the other hand, each of applicant's embodiments include a *plurality* of such memory modules. Katayama et al. do not specifically mention that memory controller 17 could be connected to *more than one* storage device 16. However, the benefits of adding extra memory were quite well known. Whether extra memory devices 16 were added in parallel, series or in some combinations thereof, it would have been obvious to one having ordinary skill in the art at the time the invention was made to add such extra devices since (1) extra memory meant that more data could be stored, (2) several storage devices 16 linked in

parallel would have allowed for faster data retrieval via parallel data transfers, and (3) it was noted in St. Regis Paper Co. v Bemis Co. 193 USPQ 8 (7th Cir. 1977) that to duplicate parts for multiple effects is *not* given patentable weight.

As for the use of sockets to connect memory modules containing a plurality of memory devices (DRAMs), this was not specifically mentioned in the Katayama et al. system. However, this feature was explicitly taught by Bechtolsheim et al. (note, e.g., the Abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the use of sockets to connect the memory "module" 16 of Katayama et al. to the memory controller 17, since this would have made connecting and disconnecting elements (for maintenance, upgrading, etc.) much faster.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 13-16 and 32-60 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 50-54 of copending Application No. 09/434,731. Although the conflicting claims are not identical, they are not patentably distinct from each other because both are now limited to the use of a single socket.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented. The prohibition against holdings of double patenting applies to requirements for restriction between the related subjects treated in MPEP 806.04 through 806.05(I), namely, between combination and subcombination thereof, between subcombinations disclosed as usable together, between process and apparatus for its practice, between process and product made by such process and between apparatus and product made by such apparatus, etc., so long as the claims in each case are filed as a result of such requirement.

Note:

The following are situations where the prohibition of double patenting rejections under 35 U.S.C. 121 does not apply: ...

(b) The claims of the different applications or patents are not consonant with the restriction requirement made by the examiner, since the claims have been changed in material respects from the claims at the time the requirement was made. For example, the divisional application filed includes additional claims not consonant in scope with the original claims which were subject to restriction in the parent. Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991); Gerber Garment Technology, Inc. v . Lectra Systems Inc., 916 F.2d 683, 16 USPQ2d 1436 (Fed. Cir. 1990). In order for consonance to exist, the line of demarcation between the independent and distinct inventions identified by the examiner in the requirement for restriction must be maintained. Gerber , supra.

Response to Amendment

10. With regard to the remarks submitted with the amendment filed January 18, 2002, these have been carefully considered but are not deemed convincing for at least the following reasons:

The some of the previous rejections have been withdrawn. New rejections have been made herein.

Applicant needed evidence to show that memory modules were connected via sockets. This evidence has been provided and incorporated into the prior art rejection above.

Applicant has provided no response to the nonstatutory double patenting rejection.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

B. James Peikari
Primary Examiner
Art Unit 2186

March 12, 2002